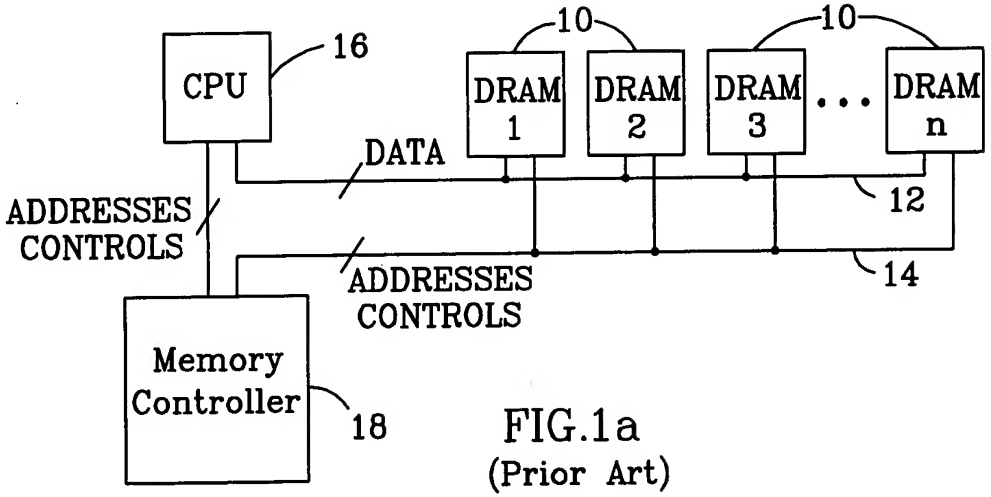


FIG.1a
(Prior Art)

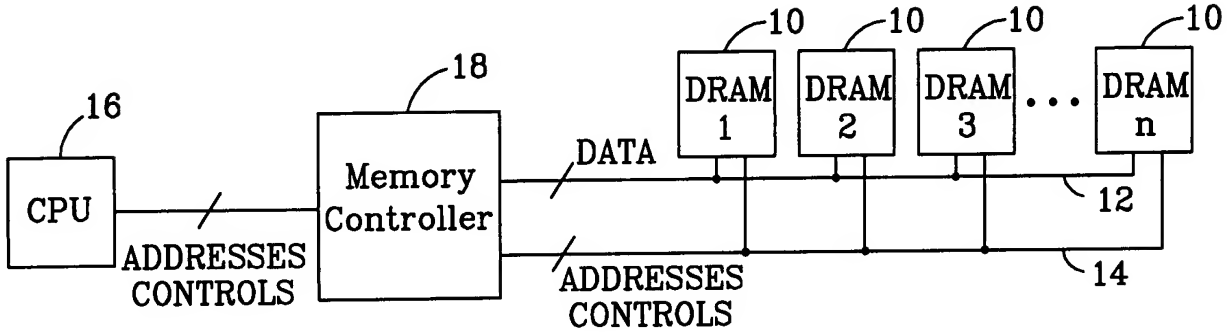


FIG.1a
(Prior Art)

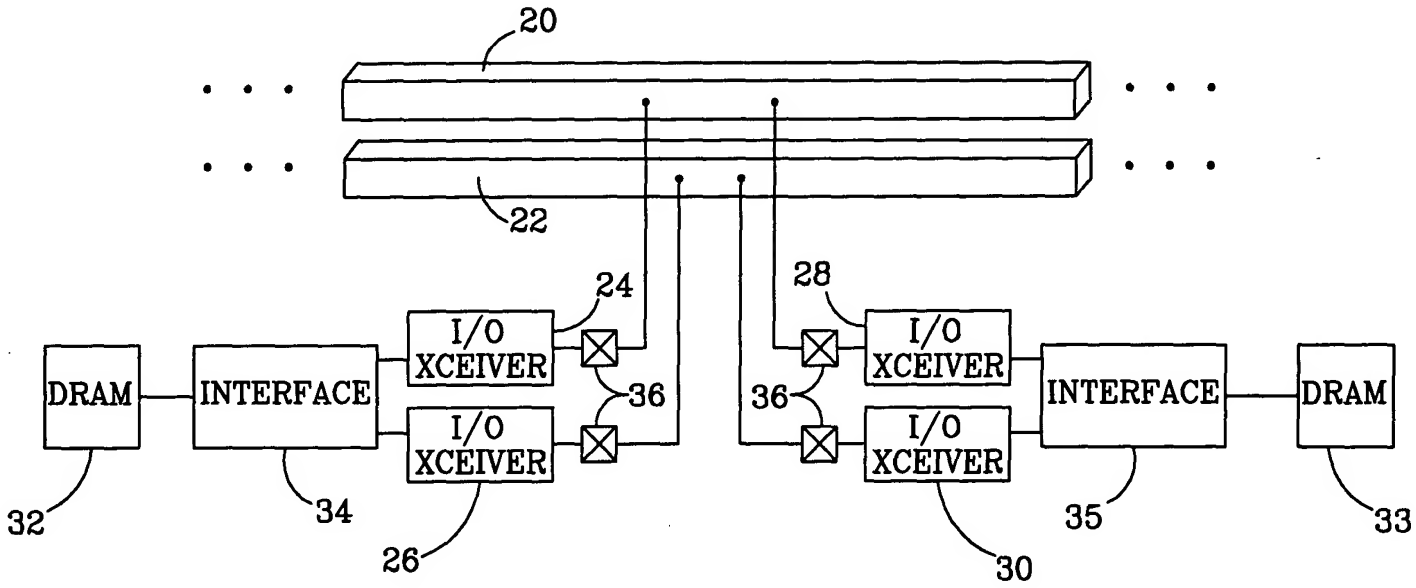


FIG.2
(Prior Art)

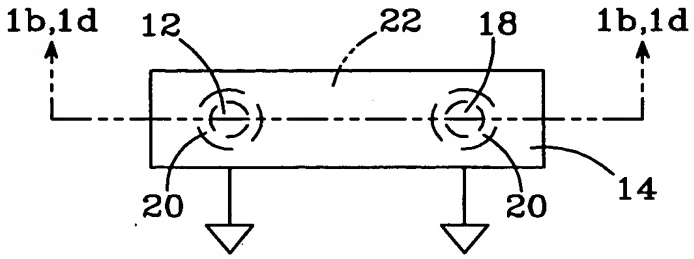


FIG.3a

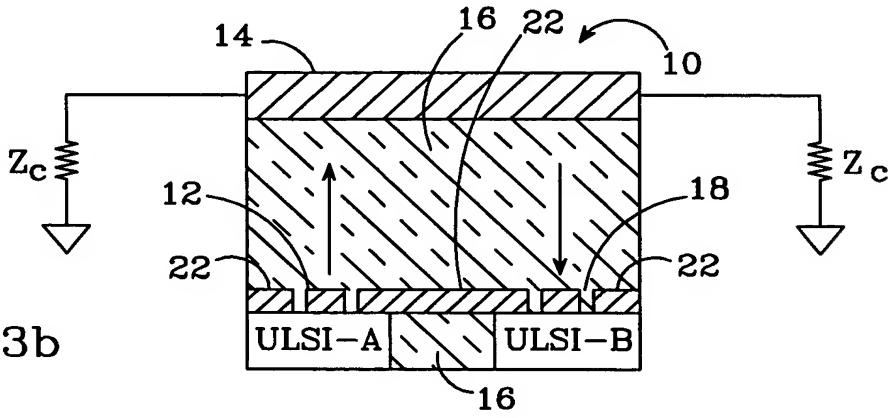


FIG.3b

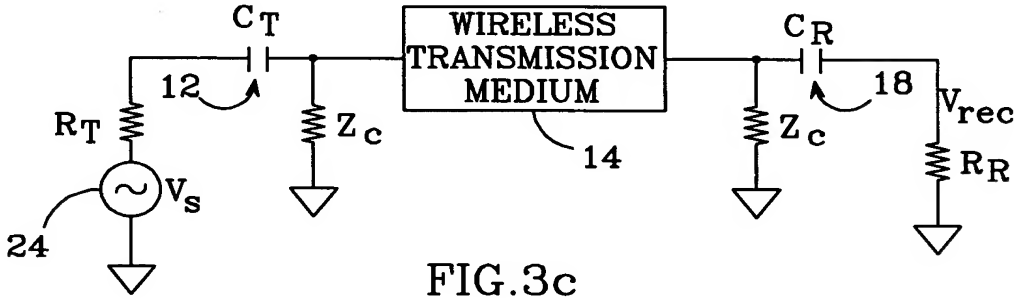


FIG.3c

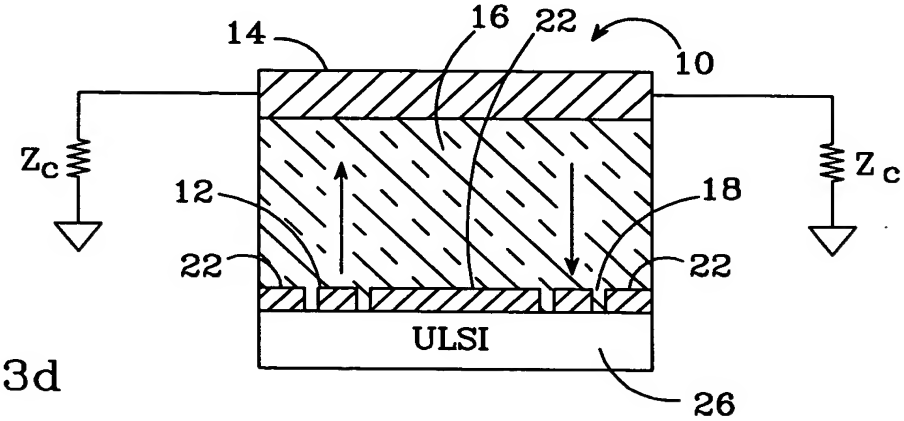


FIG.3d

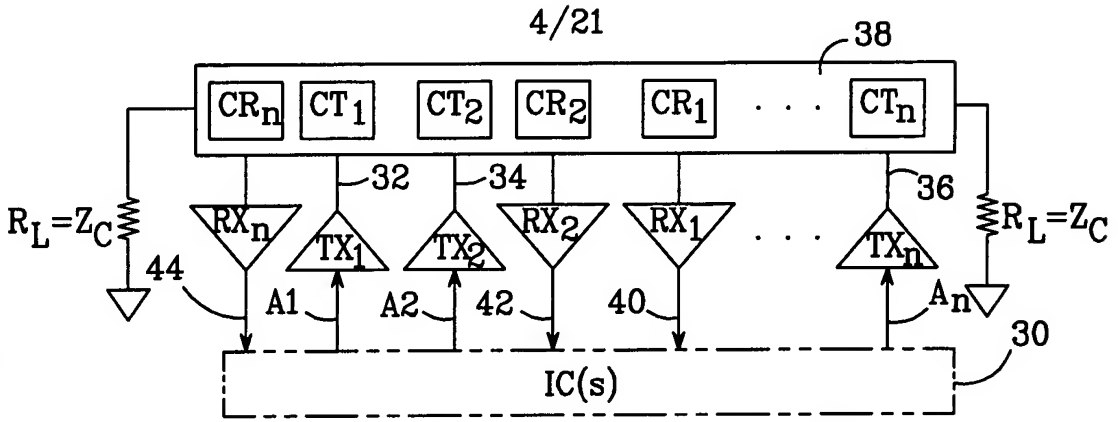


FIG.4a

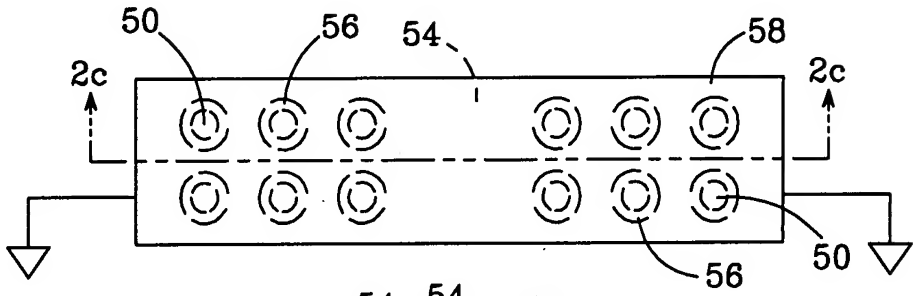


FIG.4b

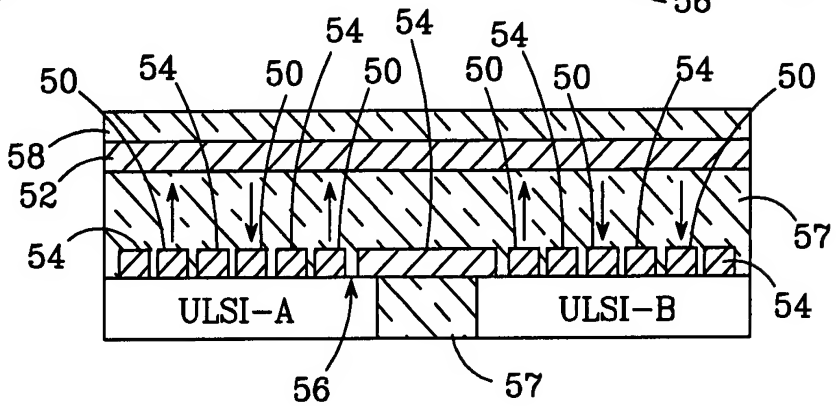


FIG.4c

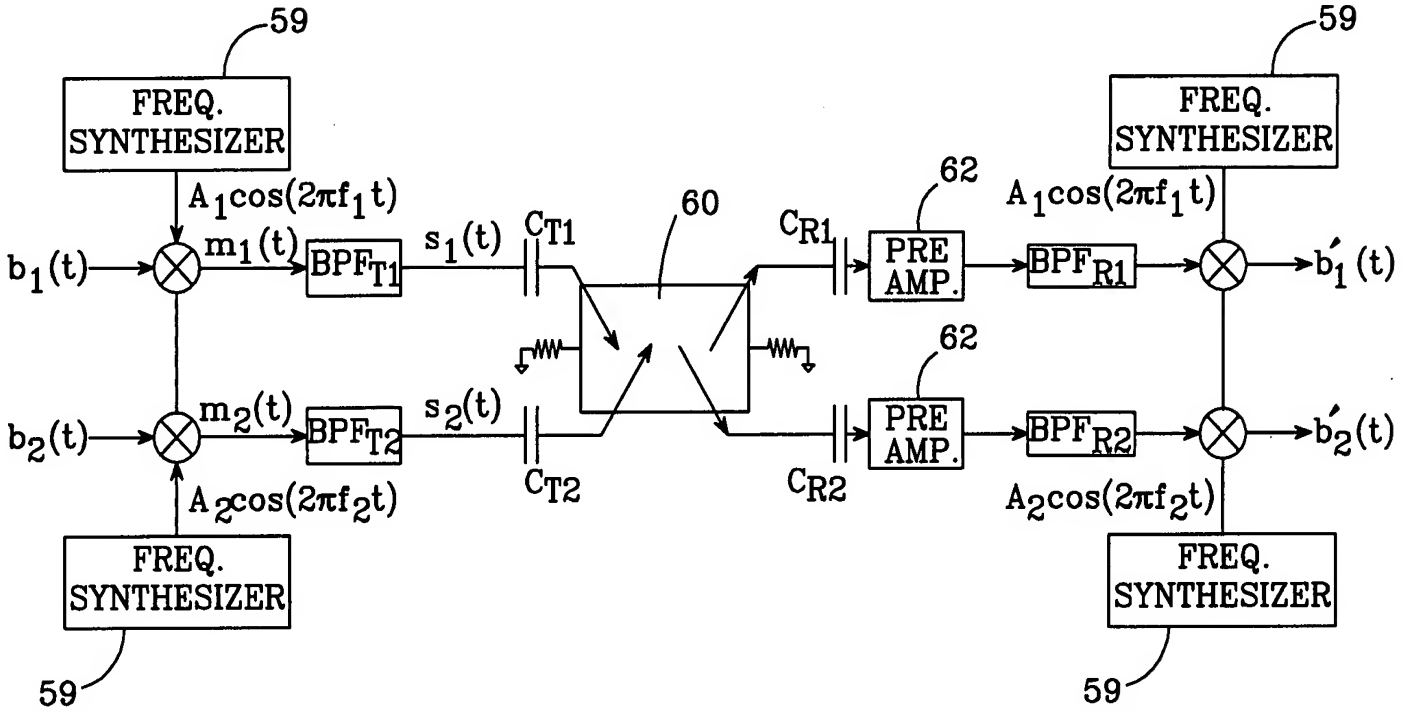

59
FREQ. SYNTHESIZER
$A_1\cos(2\pi f_1 t)$
$b_1(t)$
$m_1(t)$
BPF_{T1}
$s_1(t)$
C_{T1}
60
C_{R1}
62
PRE AMP.
BPF_{R1}
$b'_1(t)$
$b_2(t)$
$m_2(t)$
BPF_{T2}
$s_2(t)$
C_{T2}
C_{R2}
PRE AMP.
BPF_{R2}
$b'_2(t)$
$A_2\cos(2\pi f_2 t)$
FREQ. SYNTHESIZER
59

FIG.5

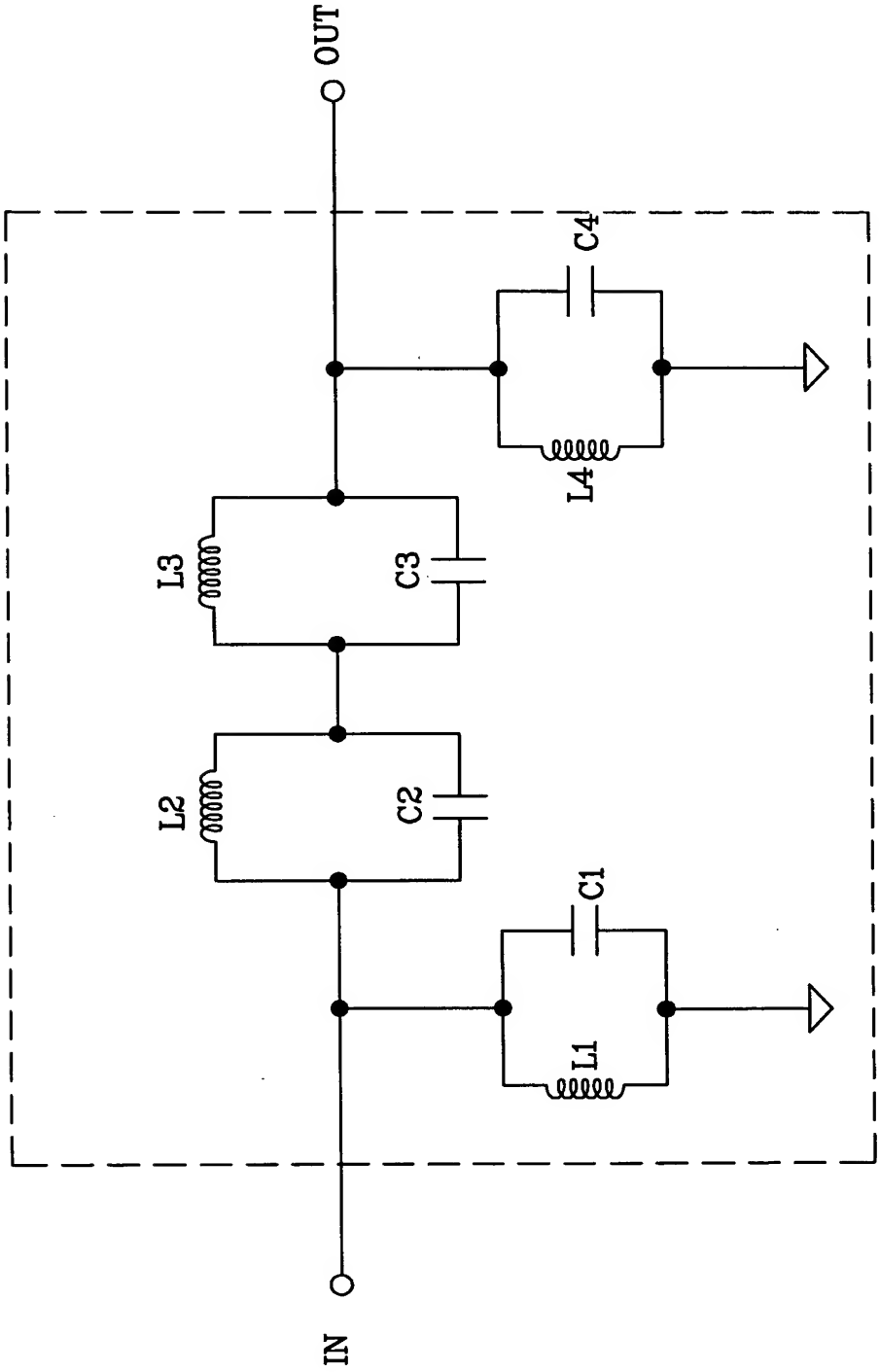


FIG.6

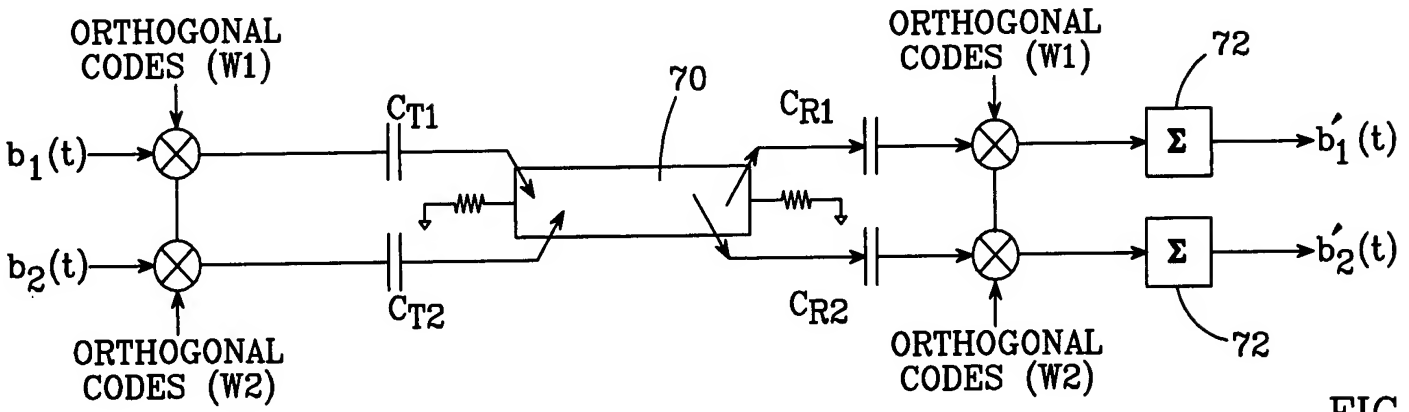

ORTHOGONAL CODES (W1)
$b_1(t)$
$b_2(t)$
ORTHOGONAL CODES (W2)
C_{T1}
C_{T2}
70
C_{R1}
C_{R2}
ORTHOGONAL CODES (W1)
ORTHOGONAL CODES (W2)
72
72
Σ
Σ
$b'_1(t)$
$b'_2(t)$

FIG.7

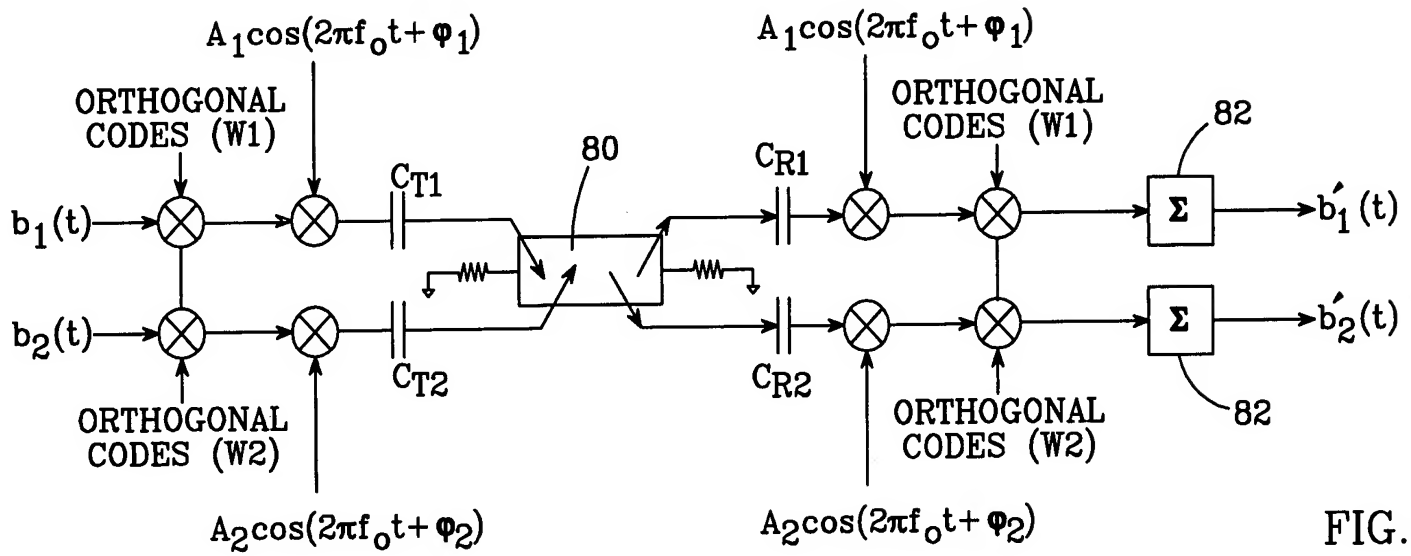

$A_1\cos(2\pi f_o t+\varphi_1)$
$A_1\cos(2\pi f_o t+\varphi_1)$
ORTHOGONAL CODES (W1)
ORTHOGONAL CODES (W1)
$b_1(t)$
$b_2(t)$
ORTHOGONAL CODES (W2)
$A_2\cos(2\pi f_o t+\varphi_2)$
$A_2\cos(2\pi f_o t+\varphi_2)$
C_{T1}
C_{T2}
80
C_{R1}
C_{R2}
82
82
Σ
Σ
$b'_1(t)$
$b'_2(t)$

FIG.8

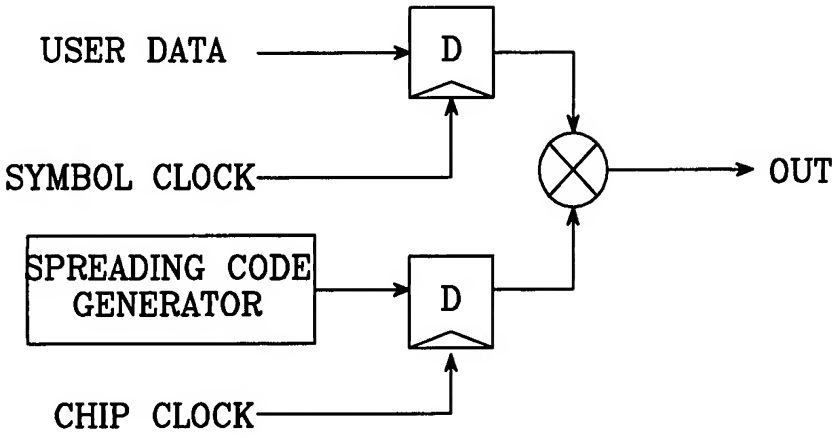

USER DATA
D
SYMBOL CLOCK
OUT
SPREADING CODE GENERATOR
D
CHIP CLOCK

FIG.9a

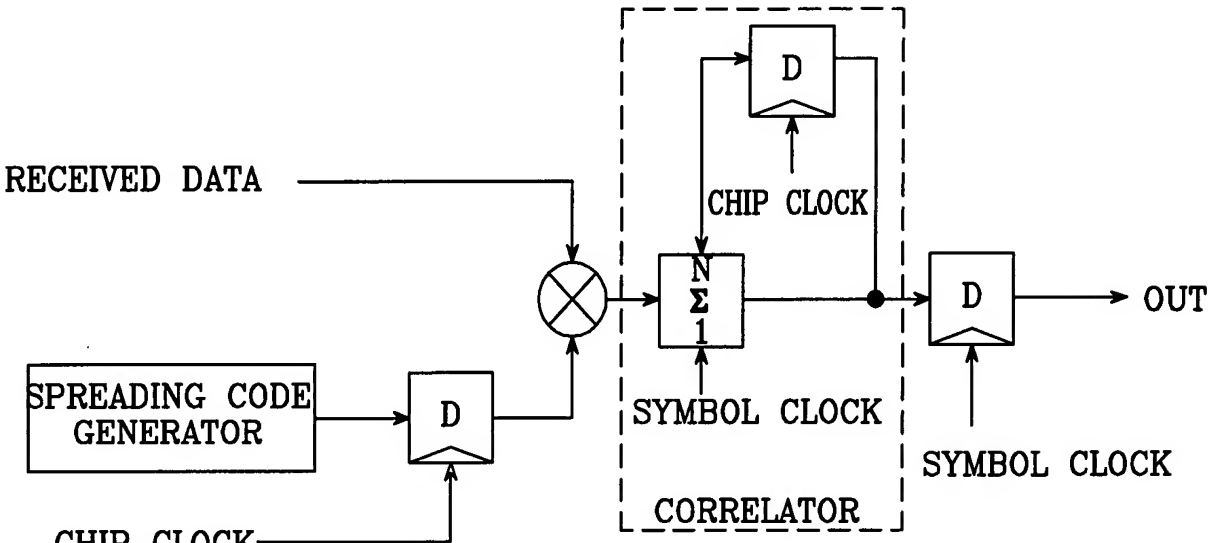

D
RECEIVED DATA
CHIP CLOCK
N
Σ
1
D
OUT
SPREADING CODE GENERATOR
D
SYMBOL CLOCK
SYMBOL CLOCK
CORRELATOR
CHIP CLOCK

FIG.9b

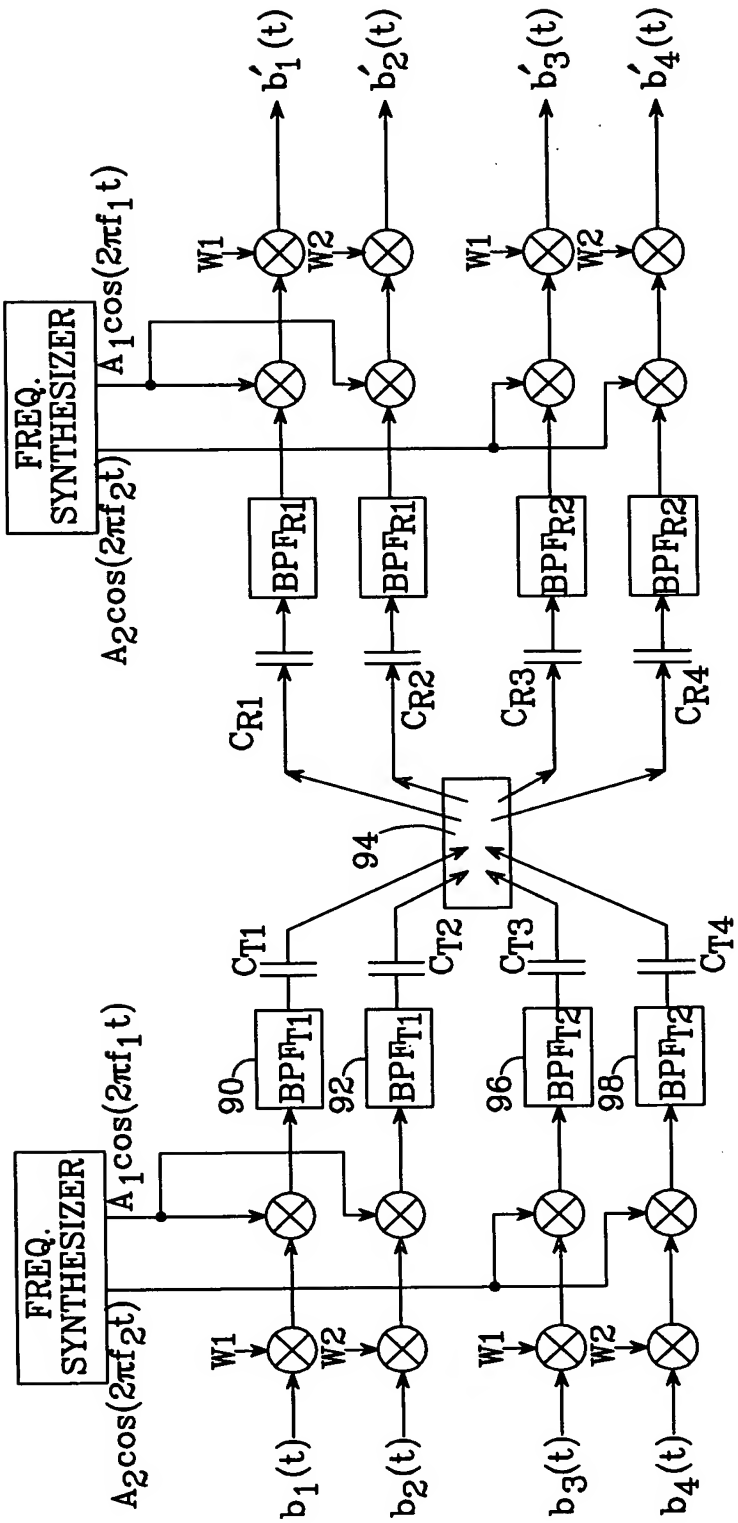

FREQ. SYNTHESIZER
$A_2\cos(2\pi f_2 t)$
$A_1\cos(2\pi f_1 t)$
$b_1(t)$
$b_2(t)$
$b_3(t)$
$b_4(t)$
W1
W2
90
92
96
98
BPF_{T1}
BPF_{T2}
C_{T1}
C_{T2}
C_{T3}
C_{T4}
94
C_{R1}
C_{R2}
C_{R3}
C_{R4}
BPF_{R1}
BPF_{R2}
$b'_1(t)$
$b'_2(t)$
$b'_3(t)$
$b'_4(t)$

FIG.10

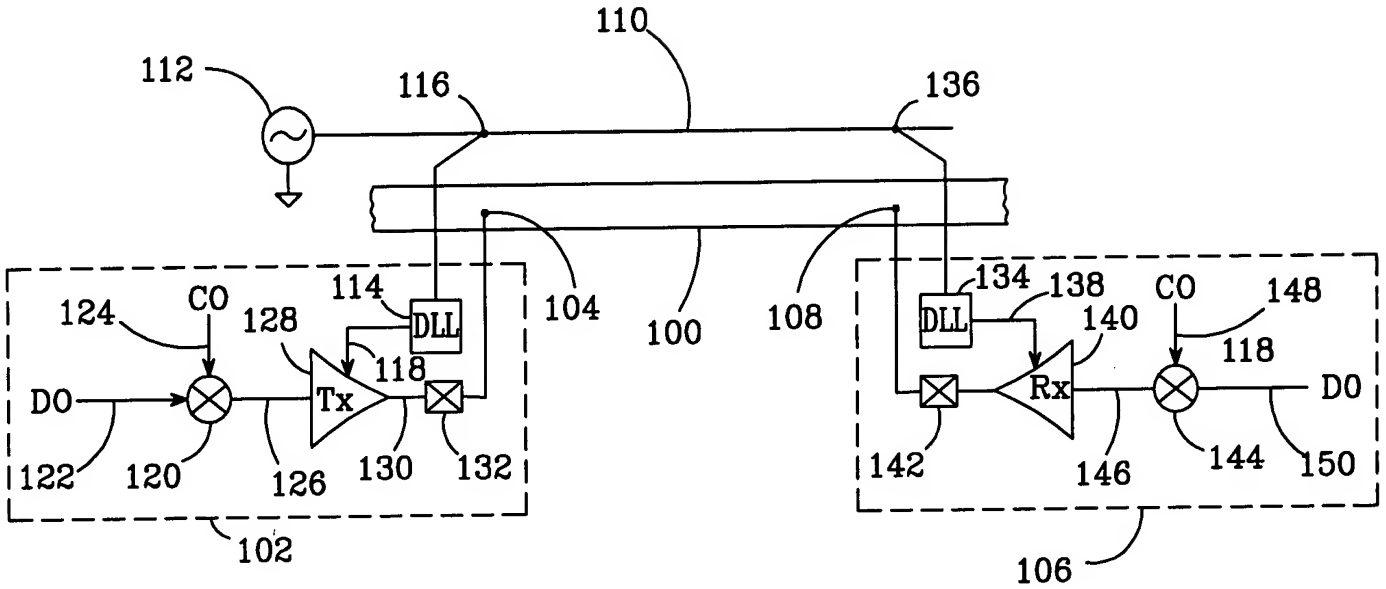

110
112
116
136
114
DLL
104
100
108
134
138
CO
148
124
CO
128
DLL
140
118
118
DO
Tx
Rx
DO
122
120
126
130
132
142
146
144
150
102
106

FIG.11

Fig. 12 a

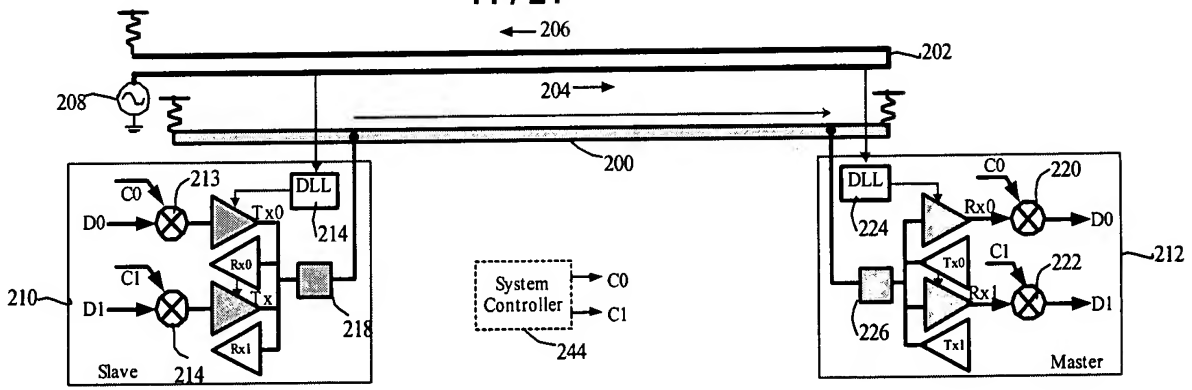


Fig. 12 b

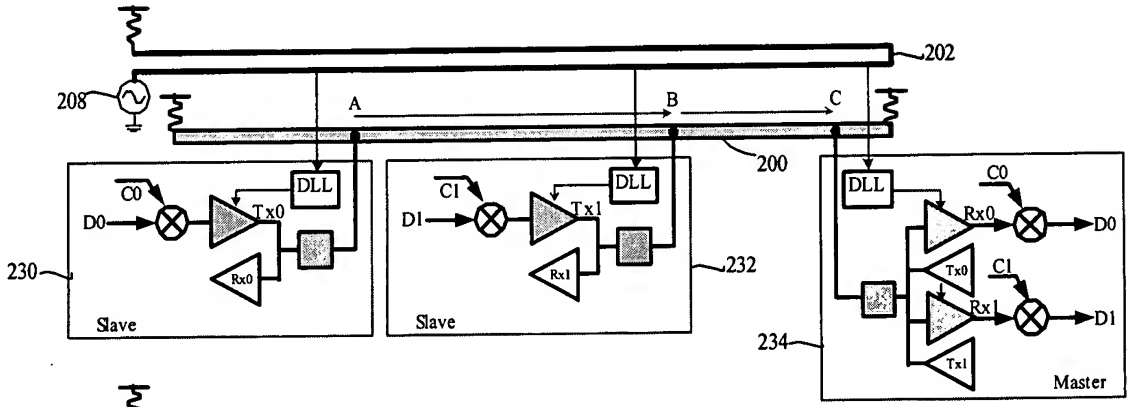
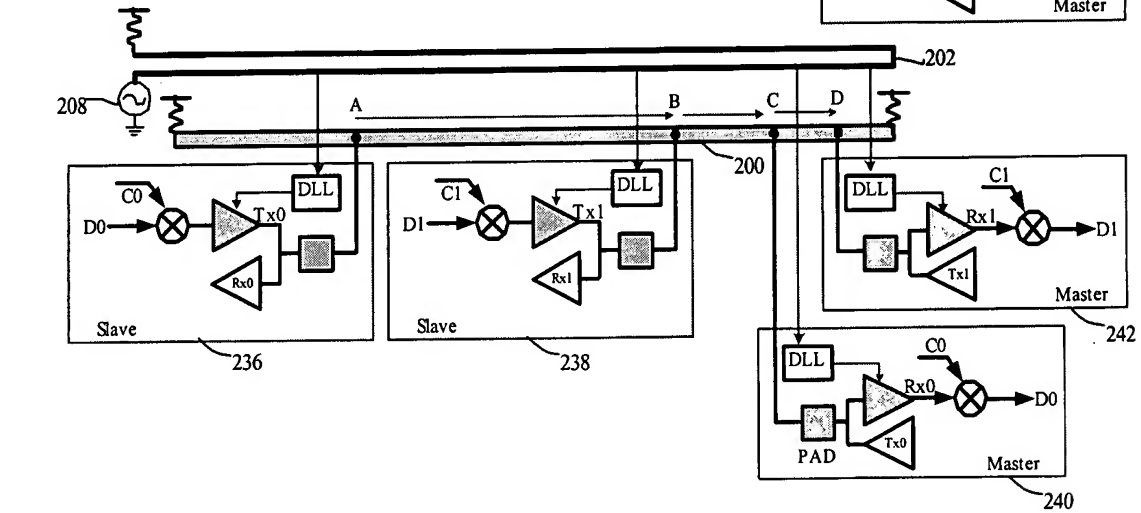


Fig. 12 c



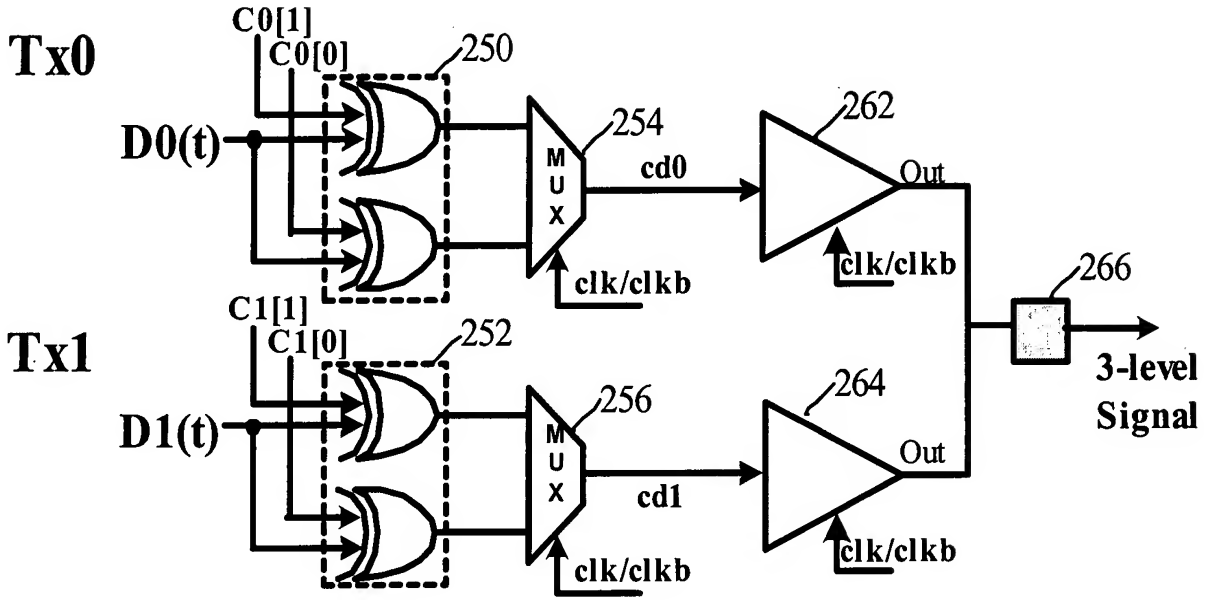

Tx0
C0[1]
C0[0]
250
D0(t)
254
MUX
cd0
clk/clkb
262
Out
clk/clkb
266
3-level
Signal
Tx1
C1[1]
C1[0]
252
D1(t)
256
MUX
cd1
clk/clkb
264
Out
clk/clkb

FIG. 13

Fig. 14 a

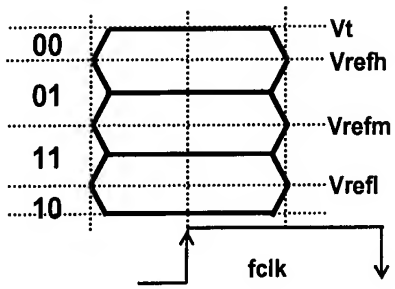
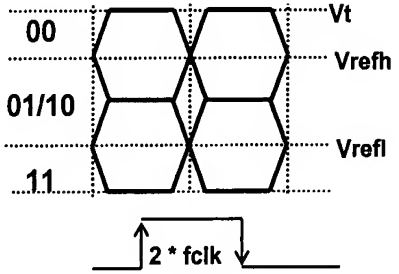


Fig. 14 b



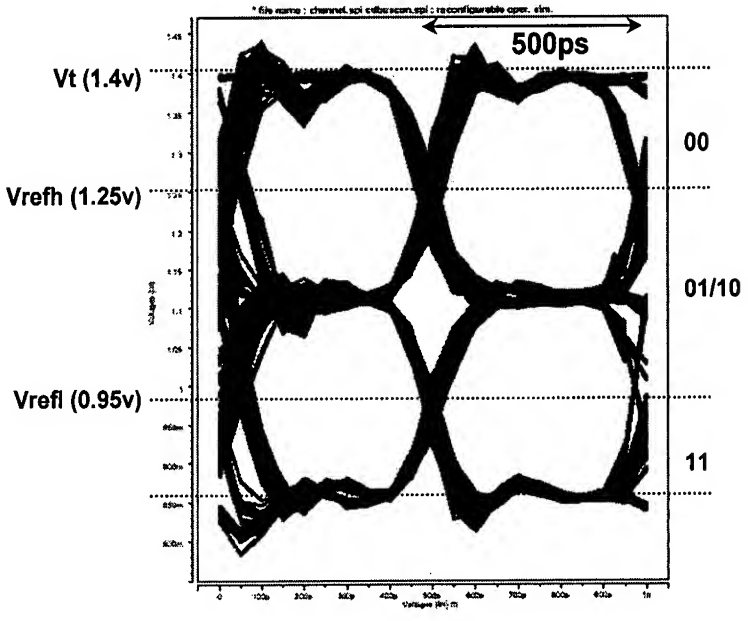


Fig. 14 c

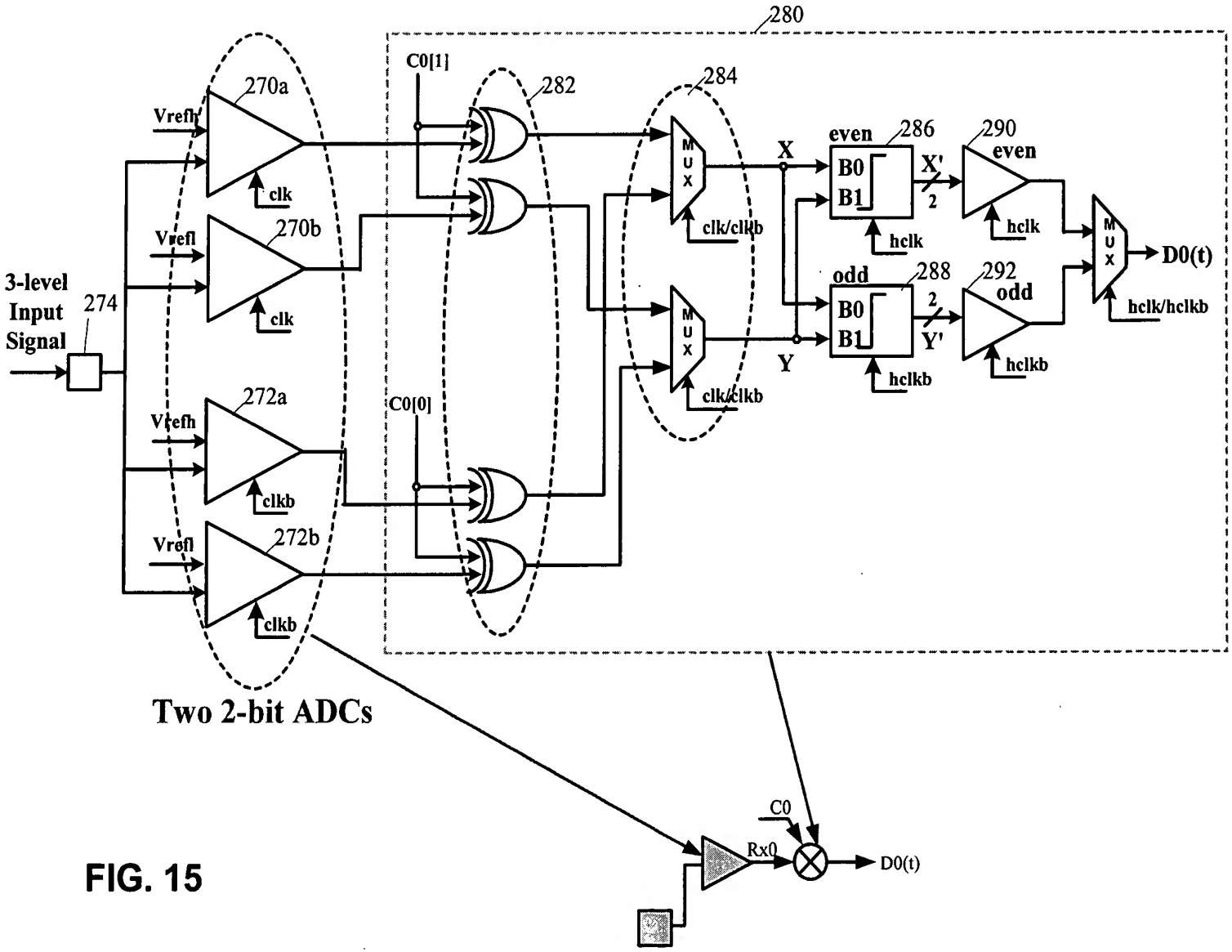

280
C0[1]
282
284
270a
Vrefh
clk
Vrefl
270b
clk
3-level
Input
Signal
274
272a
Vrefh
clkb
Vrefl
272b
clkb
C0[0]
MUX
clk/clkb
X
Y
even
286
B0
B1
hclk
X'
2
290
even
hclk
odd
288
B0
B1
hclkb
Y'
2
292
odd
hclkb
MUX
hclk/hclkb
D0(t)
Two 2-bit ADCs
C0
Rx0
D0(t)

FIG. 15

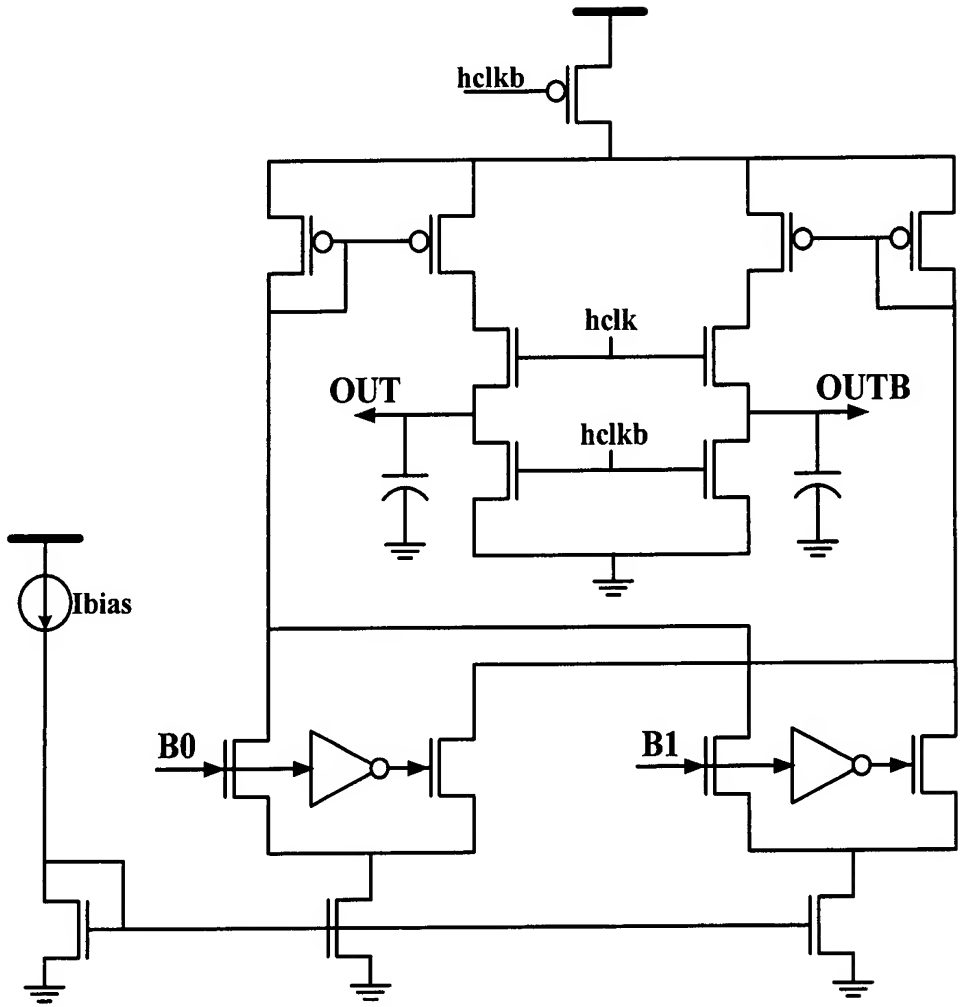


FIG. 16

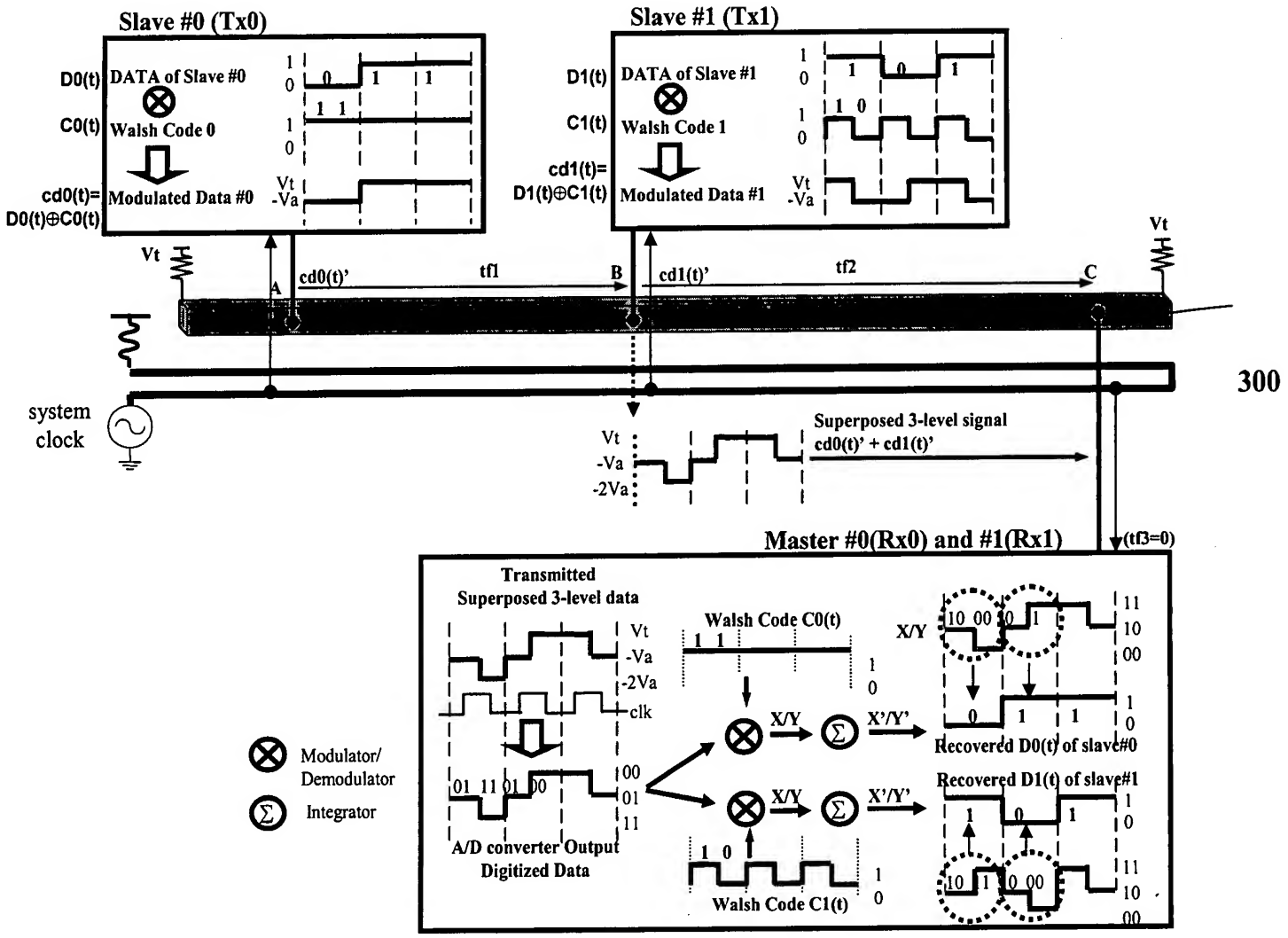

Slave #0 (Tx0)
D0(t)
DATA of Slave #0
C0(t)
Walsh Code 0
cd0(t)=
D0(t)⊕C0(t)
Modulated Data #0
Vt
-Va
Slave #1 (Tx1)
D1(t)
DATA of Slave #1
C1(t)
Walsh Code 1
cd1(t)=
D1(t)⊕C1(t)
Modulated Data #1
A
B
C
cd0(t)'
tf1
cd1(t)'
tf2
300
system
clock
-2Va
Superposed 3-level signal
cd0(t)' + cd1(t)'
Master #0(Rx0) and #1(Rx1)
(tf3=0)
Transmitted
Superposed 3-level data
clk
A/D converter Output
Digitized Data
Walsh Code C0(t)
Walsh Code C1(t)
X/Y
X'/Y'
Recovered D0(t) of slave#0
Recovered D1(t) of slave#1
Modulator/
Demodulator
Integrator

FIG. 17

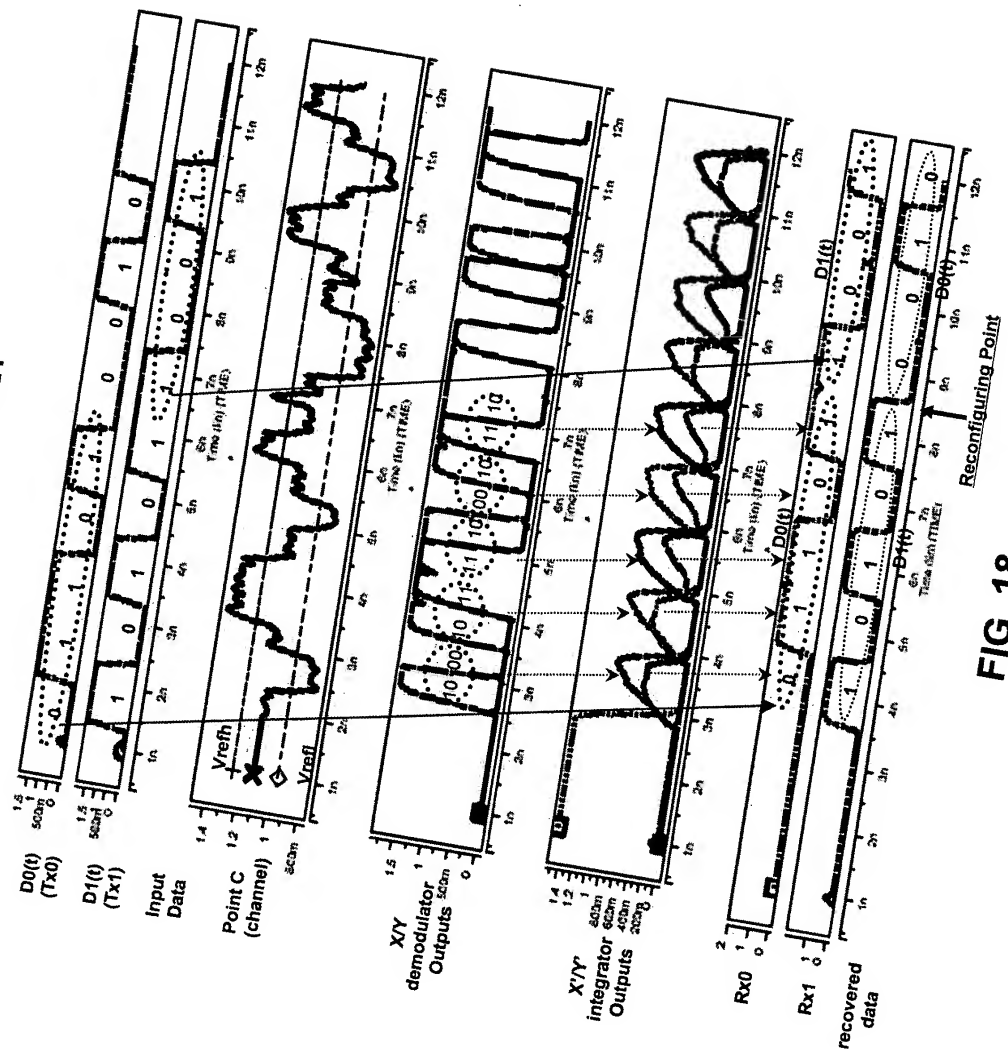
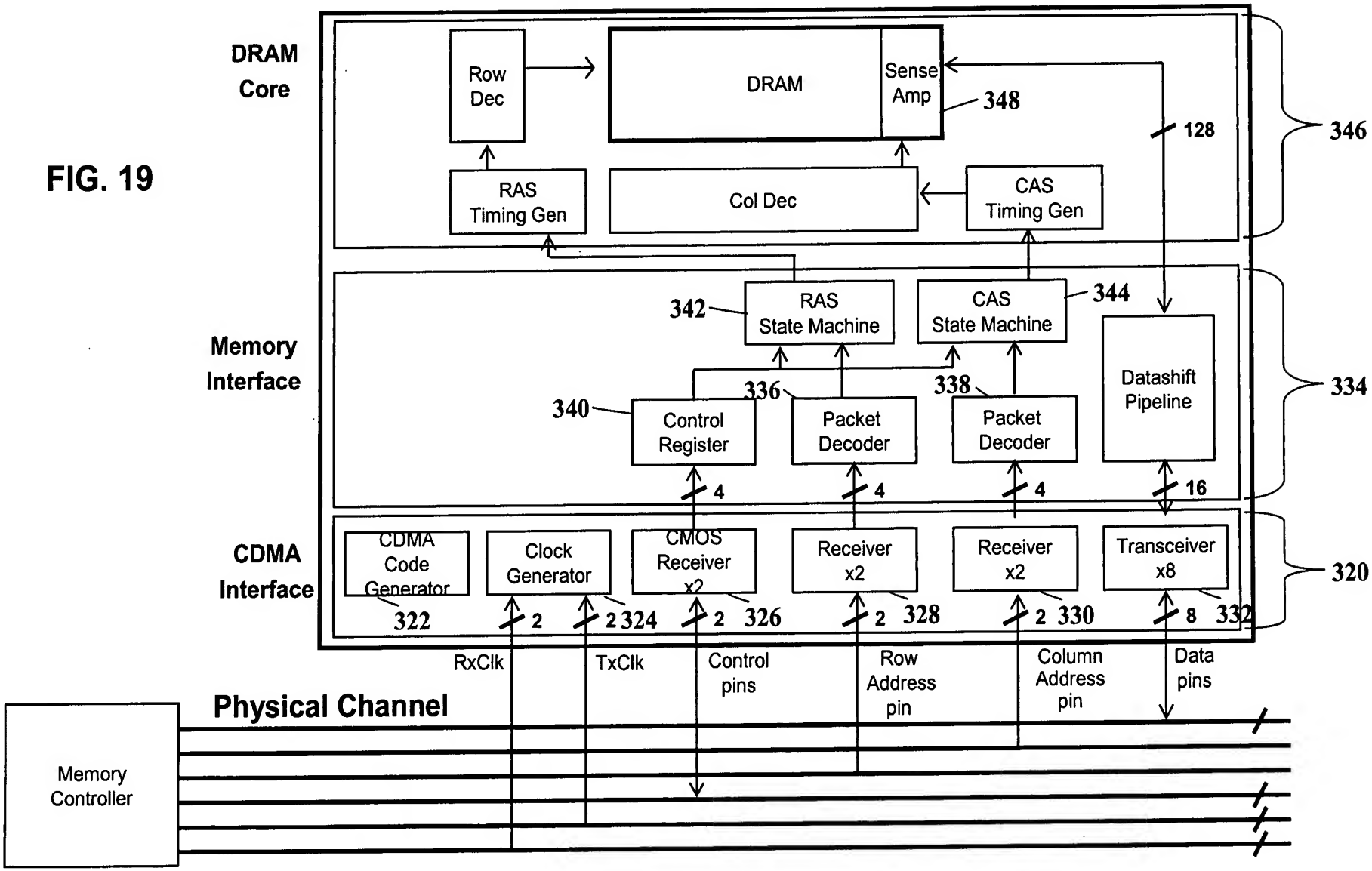

D0(t) (Tx0)
D1(t) (Tx1)
Input Data
Point C (channel)
Vrefh
Vrefl
X/Y demodulator Outputs
X'/Y' integrator Outputs
Rx0
Rx1
recovered data
D0(t)
D1(t)
Reconfiguring Point

FIG. 18

FIG. 19


DRAM Core
Row Dec
DRAM
Sense Amp
348
128
346
RAS Timing Gen
Col Dec
CAS Timing Gen
Memory Interface
342
RAS State Machine
CAS State Machine
344
Datashift Pipeline
334
340
Control Register
336
Packet Decoder
338
Packet Decoder
4
4
4
16
CDMA Interface
CDMA Code Generator
Clock Generator
CMOS Receiver x2
Receiver x2
Receiver x2
Transceiver x8
320
322
2
2 324
2
326
2
328
2
330
8
332
RxClk
TxClk
Control pins
Row Address pin
Column Address pin
Data pins
Physical Channel
Memory Controller

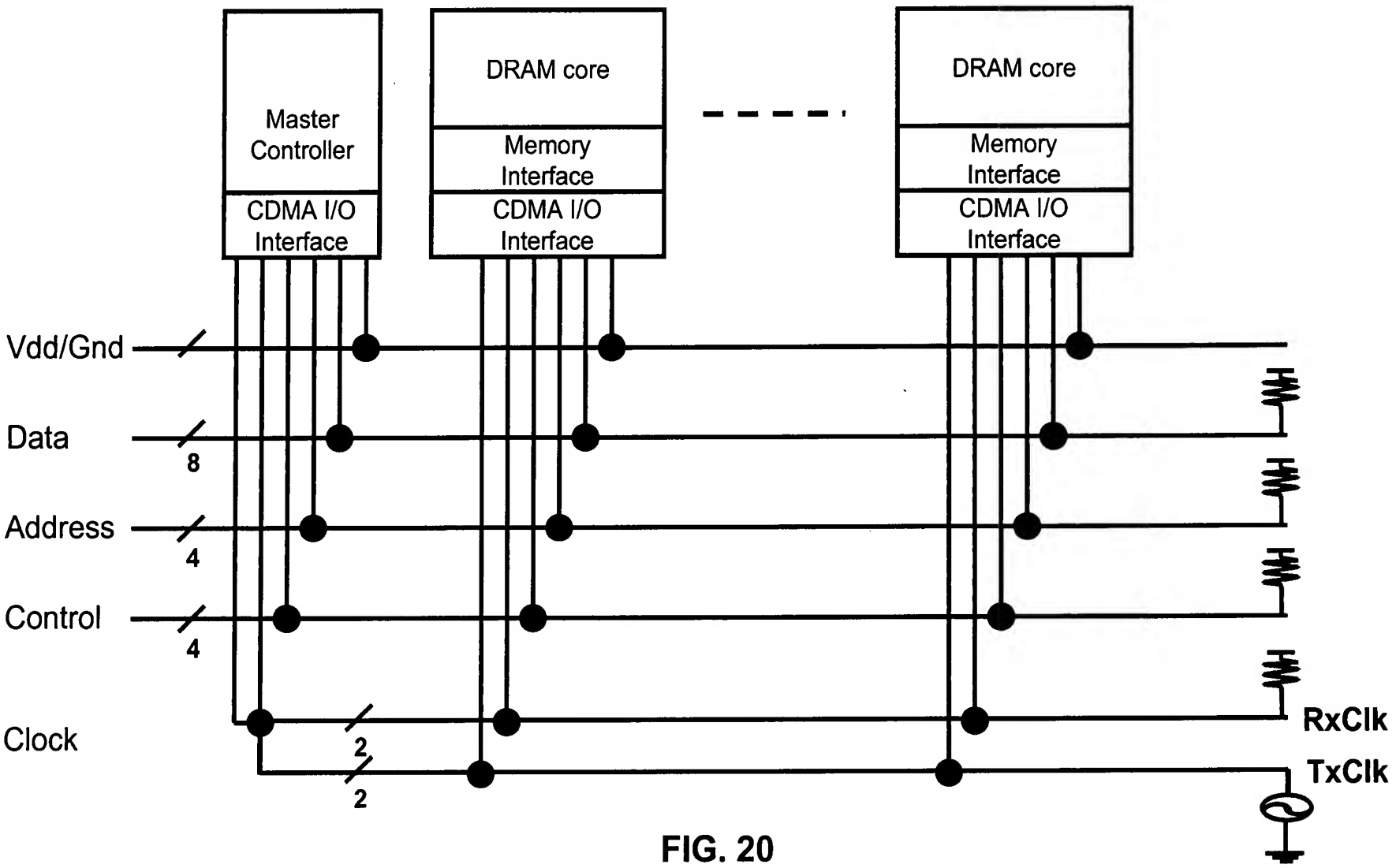
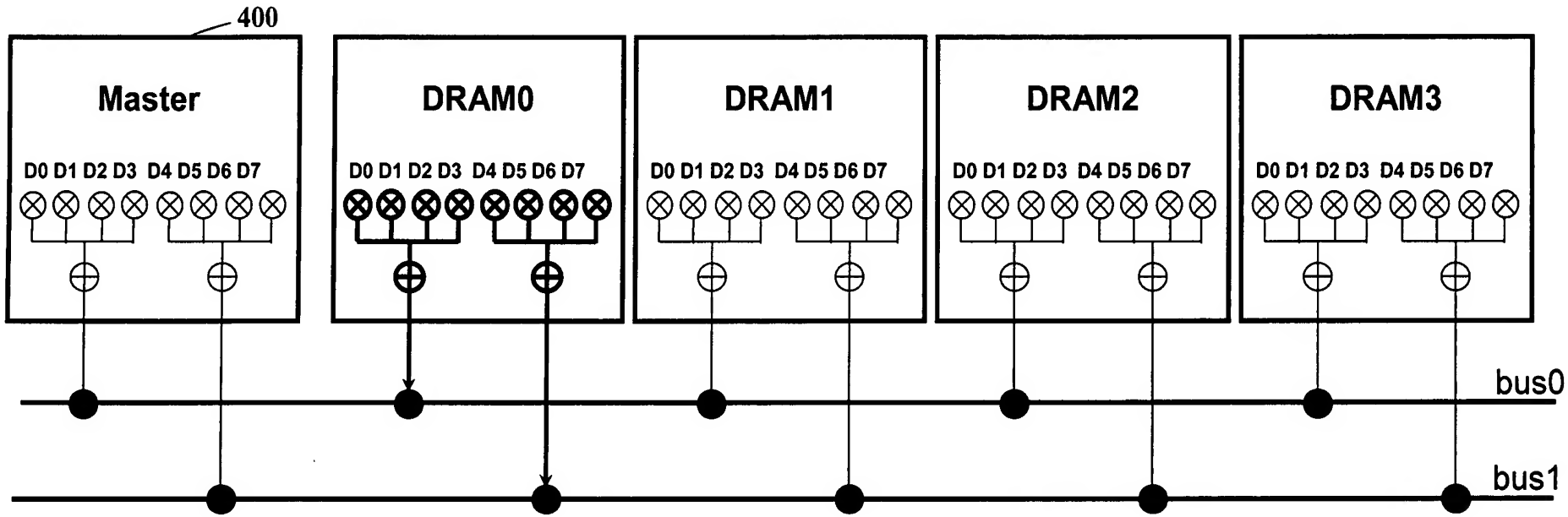
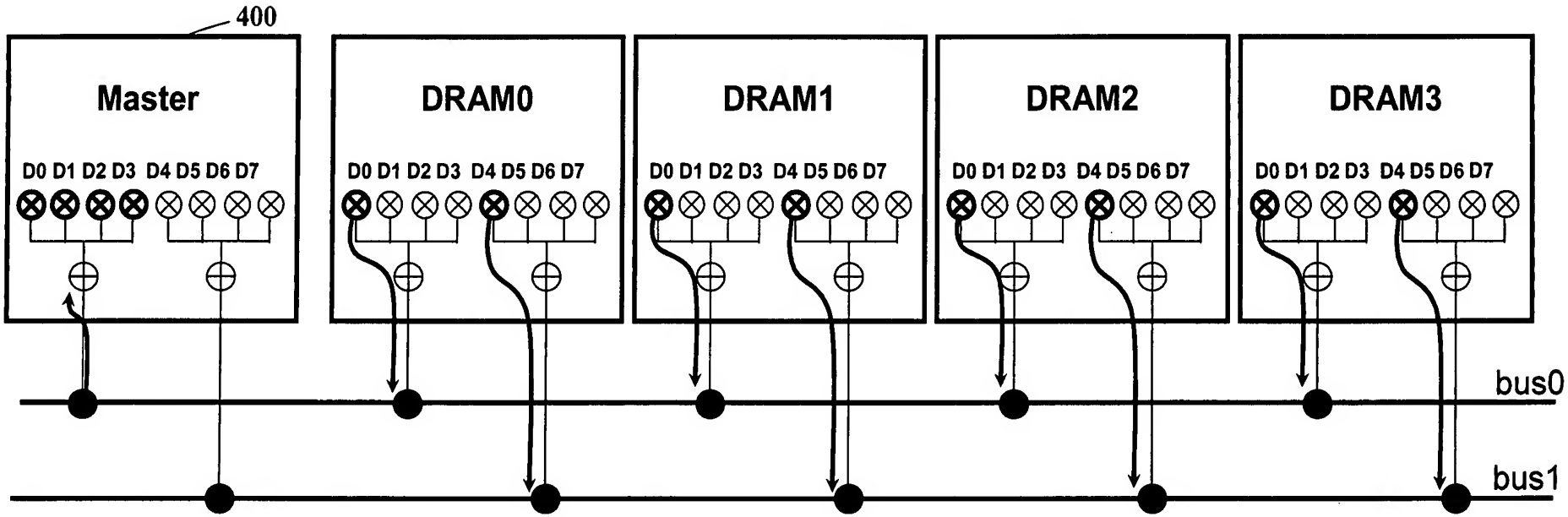

Master Controller
CDMA I/O Interface
DRAM core
Memory Interface
CDMA I/O Interface
DRAM core
Memory Interface
CDMA I/O Interface
Vdd/Gnd
Data
8
Address
4
Control
4
Clock
2
2
RxClk
TxClk

FIG. 20



DQ	CDMA Code				
	Master	DRAM0	DRAM1	DRAM2	DRAM3
D0	W0	W0	-	-	-
D1	W1	W1	-	-	-
D2	W2	W2	-	-	-
D3	W3	W3	-	-	-
D4	W4	W4	-	-	-
D5	W5	W5	-	-	-
D6	W6	W6	-	-	-
D7	W7	W7	-	-	-

FIG. 21



DQ	CDMA Code				
	Master	DRAM0	DRAM1	DRAM2	DRAM3
D0	W0	W0	W1	W2	W3
D1	W1	-	-	-	-
D2	W2	-	-	-	-
D3	W3	-	-	-	-
D4	W4	W4	W5	W6	W7
D5	W5	-	-	-	-
D6	W6	-	-	-	-
D7	W7	-	-	-	-

FIG. 22